

detecting circuit 24 and a reference voltage Vref to amplify the error therebetween. Both of these features are clearly shown in Fig. 8.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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JAO:EDM/jfb

Date: March 8, 2006

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